ROHDE&SCHWARZ

SERVICE DOCUMENTS
I/Q-Demodulator

1066.1260.02

1066.1260.02/03

1066.2520.02

Contents

7 Testing of Unit

7.1 Functional Description

7.1.1 Function in Equipment

The option vector analyzer with the I/Q demodulator board analyzes the IF signal within the set resolution bandwidth.
For evaluation, the following settings are available:

Timing
Modulation

For these measurements, the analyzer is always set to a fixed frequency (ZERO-SPAN) in the operating mode **VECTOR-ANALYZER**.

7.1.1.1 Explanation of Block Diagram

The I/Q demodulator board can be divided into two main blocks:
A) Analog unit:

1) IF amplifier/conversion from 21.4 MHz to 6.4 MHz or 1.4 MHz
2) Clock conditioning for A/D converter and digital mixer and filter devices

B) Digital unit:

1) Digital down-conversion of the IF signal into I and Q signals in baseband position and subsequent data reduction and filtering.
2) Further processing of the digital data in two DSPs and routing of the preprocessed I and Q data via the serial DSP interface to further DSPs (and then to the level transputer) on the detector board.

Analog unit
In order to achieve a high intermodulation-free range, the IF level is reduced for the IQ demodulator on the IF-filter board in comparison with analyzer operation. The 21.4-MHz signal is converted to 6.4 MHz or 1.4 MHz. The narrowband modulation types are processed at the 1.4-MHz IF, the broadband modulation types at the 6.4-MHz IF.
The A/D converter is operated with an adjustable clock signal and matched to the modulation frequency. To this end, the VCO is detuned in a range of approx. 25 %. Larger frequency variations are implemented by various data-reduction factors.

Digital unit
The intermediate frequency down-converted from 21.4 MHz to 6.4 and 1.4 MHz is sampled with an accuracy of 10 bits (sampling rate of AD converter can be adjusted from 20 to 26 MHz).
This 10-bit word is passed on to an integrated digital mixer (NCOM).
This input data word of the NCOM is multiplied by the intermediate frequency (ohmic multiplication) in the NCOM in two separate multipliers (once with $\sin(\omega_{IF}t)$ and once with $\cos(\omega_{IF}t)$).
After rescaling, these two NCOM output data words represent the I-signal and the Q-signal in the baseband.

As the data rate is the same as that used for sampling the IF whereas the useful information has been shifted from IF to baseband position, there is a redundancy in the number of sampling values. For this data reduction, an integrated digital filter and a data-reduction device (DDF) are used for I and Q each.

7.2 Test Equipment and Tools

No.	Name	Required specifications	Suitable R&S unit	Ordering code	Use
1	Digital multimeter	1 mV to 100 V 0.1 mA to 2 A	UDS5	349.1510.02	
2	Spectrum analyzer	100 kHz to 7 GHz	FSEB 20	1066.6000.20	

7.2.1 Selftest

6 selftest voltages can be measured on the unit. These voltages are measured in the automatic selftest for certain equipment settings and checked for adherence to specified tolerances.

Note: *The automatic selftest of this unit requires proper functioning of all analog units as well as of the digital part. Automatic testing of the complete set is always terminated after detection of the first out-of-tolerance state to avoid any inapplicable and superfluous error messages.*

The basic setting for the I/Q demodulator and that for the particular test function are generated automatically. The measured selftest voltage and the permissible tolerances appear on the analyzer display.

7.2.2 Calibration

Within the scope of calibration, the level displays are measured in I/Q-demodulation mode using the function MAGNITUDE CAPTURE BUFFER and set to the nominal value by means of the variable gain on the IF-filter board. Proper functioning of the calibration therefore requires proper functioning of all analog boards in the signal path.

2.24.2:

2.24.1.8:
1.1:
1.2:
1.3:
1.4:
1.5:
1.6:
1.7:

7.3 Troubleshooting

The following details will help you to pinpoint a fault in the Tracking Generator. Replace the unit if it is faulty.

Unit replacement

- The automatic selftest must run without error after unit replacement. In addition, the full calibration must be completed successfully without FAILED-messages.

7.3.3 Failures in the I/Q Demodulator

To ensure correct functioning of the I/Q demodulator, the following signals must be okay:

- a reference signal with 120 MHz, 8dBm must be applied to the unit via socket X173.
- an IF-signal of 21.4 MHz must be applied to the unit via socket X172.

7.3.3.1 Error messages in the selftest

To be able to determine in the instrument whether the IQ-demodulator board is faulty, the selftest can be called up (even in the uncalibrated state).

The selftest can be aborted with the following error messages:

1. **IQ-Board analog HW befor ADC**
2. **IQ-Board ADC**
3. **IQ-Board level**
4. **IQ-Board demodulation**
4. **IQ-Board irpt msg cntrl**

Should one of these error messages appear, check the following settings:

PRESET
MODE *VECTOR ANALYZER*
Switch on *DIGITAL STANDARDS GSM-Demodulator*
Switch on ***SETUP*** *SERVICE INPUT CAL*
Switch on ***MODE*** *MEAS RESULT MEAS SIGNAL*
Set ***CENTER***-Frequency to 120,0667 MHz.
UNLD must appear
Set ***REF*** REF-LEVEL to -38 dBm → 21.4 MHz IF ≈ -25 dBm
No error message may appear
Set ***REF*** REF-LEVEL to -52 dBm
IFOVLD must appear
Set ***REF*** REF-LEVEL I to -38 dBm
Switch on ***MODE*** *MEAS RESULT MAGNITUDE CAP BUFFER*
Set ***CAL*** *CAL CORR OFF*
Switch on *MKR⇒*
The level must lie in the range -35 dBm to -46 dBm

7.3.3.2 Error in the Calibration

The calibration results can be obtained from the list *CAL RESULTS (righthand side menu CAL)*. The list contains the following entries with respect to the I/Q demodulator:
IQ Level, Corr Val;
LC Filter x.xx dB PASSED
XTAL Filter x.xx dB PASSED
rel diff NORMAL x.xx dB PASSED
rel diff LOW NOISE x.xx dB PASSED

If one or more values are marked with FAILED in these lines of the list *CAL RESULTS*, the input level of the I/Q-demodulator board should be checked:

Test setup:

Remove plug from X172 and connect to spectrum analyzer.

Measurement:

Setting:

PRESET
Switch on ***SETUP*** *SERVICE INPUT CAL*
Set ***REF*** *REF LEVEL* -10 dBm
MODE *VECTOR ANALYZER*
Switch on *RESULT MAGNITUDE CAP BUFFER*
Set ***CENTER*** frequency to 120 MHz.

Measure input level: 21.4 MHz, - 44 ± 4 dBm
Switch on ***INPUT*** *ATTEN AUTO LOW NOISE*
Measure input level: 21.4 MHz, - 34 ± 4 dBm
Switch on ***INPUT*** *ATTEN AUTO LOW DISTORTION*
Measure input level: 21.4 MHz, - 54 ± 4 dBm

If all level values are within the tolerance, the error can be assumed to lie in the I/Q-demodulator board. Replace the board.

7.4 Testing Characteristics

7.4.1 Reference feedtrough

Test setup: - Connect spectrum analyzer to X174.

Test:
Settings:
- Span zero
- Measure output signal: 120 MHz, 8 ± 2 dBm

7.4.2 Demodulation test

The following test checks whether the error of the I/Q demodulator lies within the permissible tolerance.
Measurement:

Setting:

PRESET
Switch on ***SETUP*** *SERVICE INPUT CAL*
MODE *VECTOR ANALYZER*
Set ***CENTER*** frequency to 120.0667 MHz.
Set ***REF*** REF-LEVEL to -30 dBm
Switch on ***MODE*** *DIGITAL STANDARDS* GSM demodulator
Switch on ***MODE*** *MEAS RESULT SYMB TABLE / ERRORS*

Check that the display of the phase error is < 1° rms.

7.5 External Interfaces

Signal Name Description	R	A	Value	P T	Connection Point	Remark
TP_CLK	E	D	TTL		X170 A7	Clock from FTP
TP_CLKR	A	D	TTL		X170 A9	Clock to FTP
TP_DAT	E	D	TTL		X170 C7	Data from FTP
TP_DATR	E	D	TTL		X170 C8	Data to FTP
TP_STR_ADR	E	D	TTL		X170 A8	Adress strobe
TP_STR_DAT	E	D	TTL		X170 C9	Data strobe
TP_SCL	B	D	TTL 100 kHz		X170 C25	I^2C-BUS
TP_SDA	B	D	TTL 100 kHz		X170 C24	I^2C-BUS
SC1	E	D	TTL		X170 B15	DSP interface (SCI)
SC2	E	D	TTL		X170 B19	DSP interface (SCI)
SCK	E	D	TTL		X170 B16	DSP interface (SSI)
SRD	E	D	TTL		X170 B18	DSP interface (SSI)
STD	A	D	TTL		X170 B25	DSP interface (SSI)
SCLK	E	D	TTL		X170 B26	DSP interface (SSI)
RXD	E	D	TTL		X170 B28	DSP interface (SSI)
TXD	A	D	TTL		X170 B27	DSP interface e (SSI)
DSP_HREQ	A	D	TTL		X170 B13	DSP interface (HOST)
READY	E	D	TTL		X170 A1	
+28VA	E	V	28 V ± 1V	P	X170 C28	+28VA supply
-15VA	E	V	-15 V ±0.1 V	P	X170 A29,B29,C29	-15VA supply
+15VA	E	V	+15 V ± 0.1 V	P	X170 A30,B30,C30	+15VA supply
+5VA	E	V	5.5 V ± 0.05 V	P	X170 A31,B31,C31	+5 VA supply
+5VD	E	V	5.0 V ± 0.25 V	P	X170 A6,B6,C6	+5VD supply
GNDA	B	V	0 V ± 10 mV	P	X170 A2,B2,C2	Analog ground
GNDA	B	V	0 V ± 10 mV	P	X170 A3,B3,C3	Analog ground

GNDA	B	V	0 V ± 10 mV	P	X170 A32,B32,C32	Analog ground
GNDD	B	V	0 V ± 20 mV	P	X170 A4,B4,C4	Digital ground
GNDD	B	V	0 V ± 20 mV	P	X170 A5,B5,C5	Digital ground
ADC_MUX	A	A	-5VA ... +5VA		X170 A25	Selftest channel
I/Q_AF	A	A	-1V ... +1V		X170 C19	AF signal
SWP_END_I/Q	A	D	TTL		X170 C15	Data reading end
IF_OVR	A	D	TTL		X170 A20	Overrange detector (ADC-OR)
IF_OVR-10	A	D	TTL		X170 A21	Overrange detector (6dB under MSB)
INTRES	E	D	TTL		X170 A24	Overrange reset
SYNC0	B	D	TTL		X170 B20	Det-board (=trigger signal;)
SYNC1	B	D	TTL		X170 B11	Det-board
SYNC2	B	D	TTL		X170 B21	Det-board
SYNC3	B	D	TTL		X170 B12	Det-board

IF_OUT	A	A	21.4 MHz, B=RBW, Pmax=-3 dBm	P	X171	buffered IF outp.
IF_IN	E	A	21.4 MHz,Pmax=-3 dBm	P	X172	IF input (from IF filter)
120MHZ_IN	E	A	120 MHz (P ≈ +8 dBm)		X173	120-MHz reference (Fracsyn)
120MHZ_OUT	A	A	120 MHz (P ≈ +8 dBm)		X174	120-MHz reference; to 2nd IF-Conv. board)
AF_OUT	A	A	-1 V .. +1 V (fc = 20 kHz)		X177	AF signal (=I/Q_AF);
ADC_CLK_OUT	A	D	20 - 26 MHz, TTL (high-impedance;		X178	ADC-Clock Outp.

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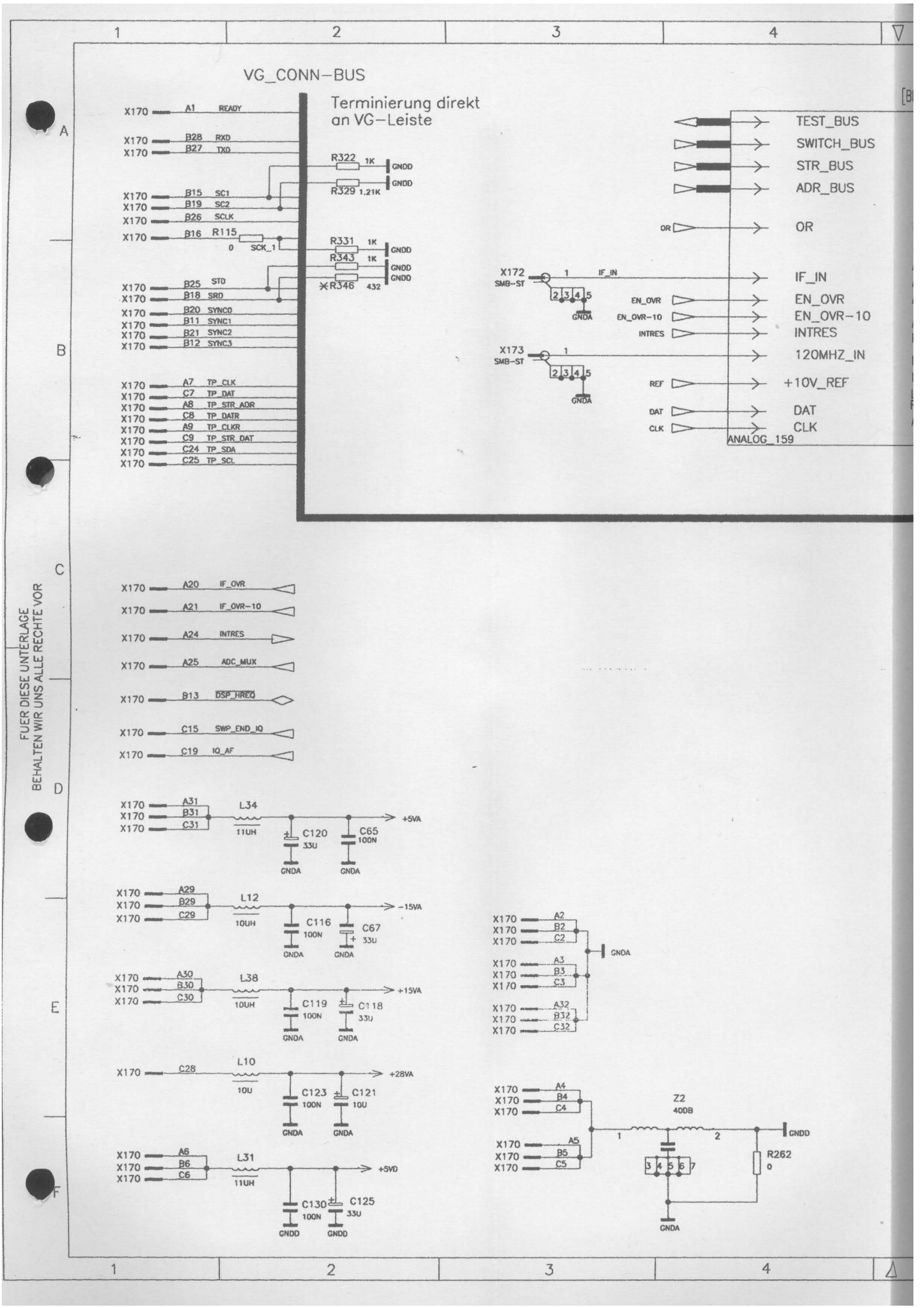
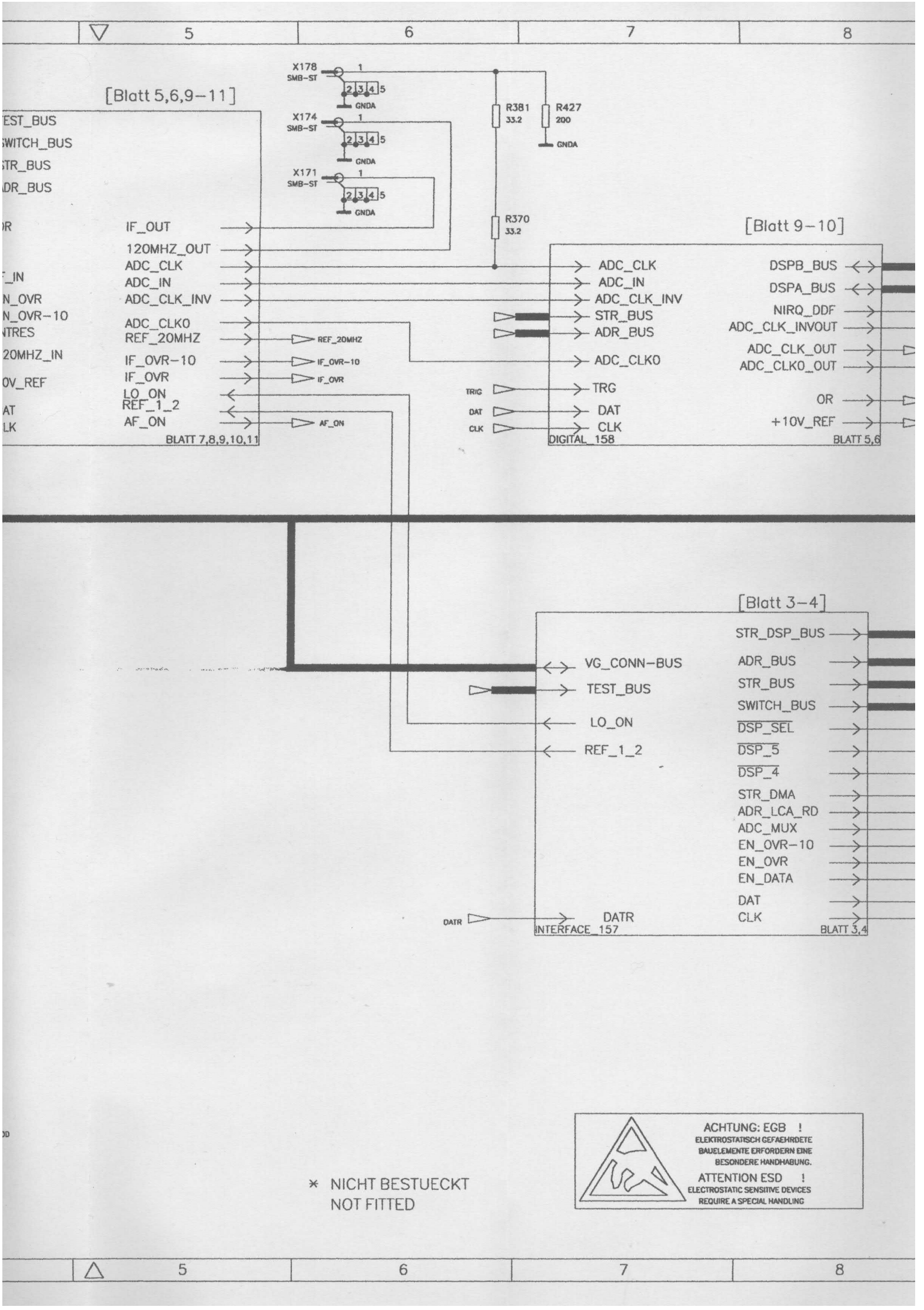
Stromläufe
Bestückungspläne

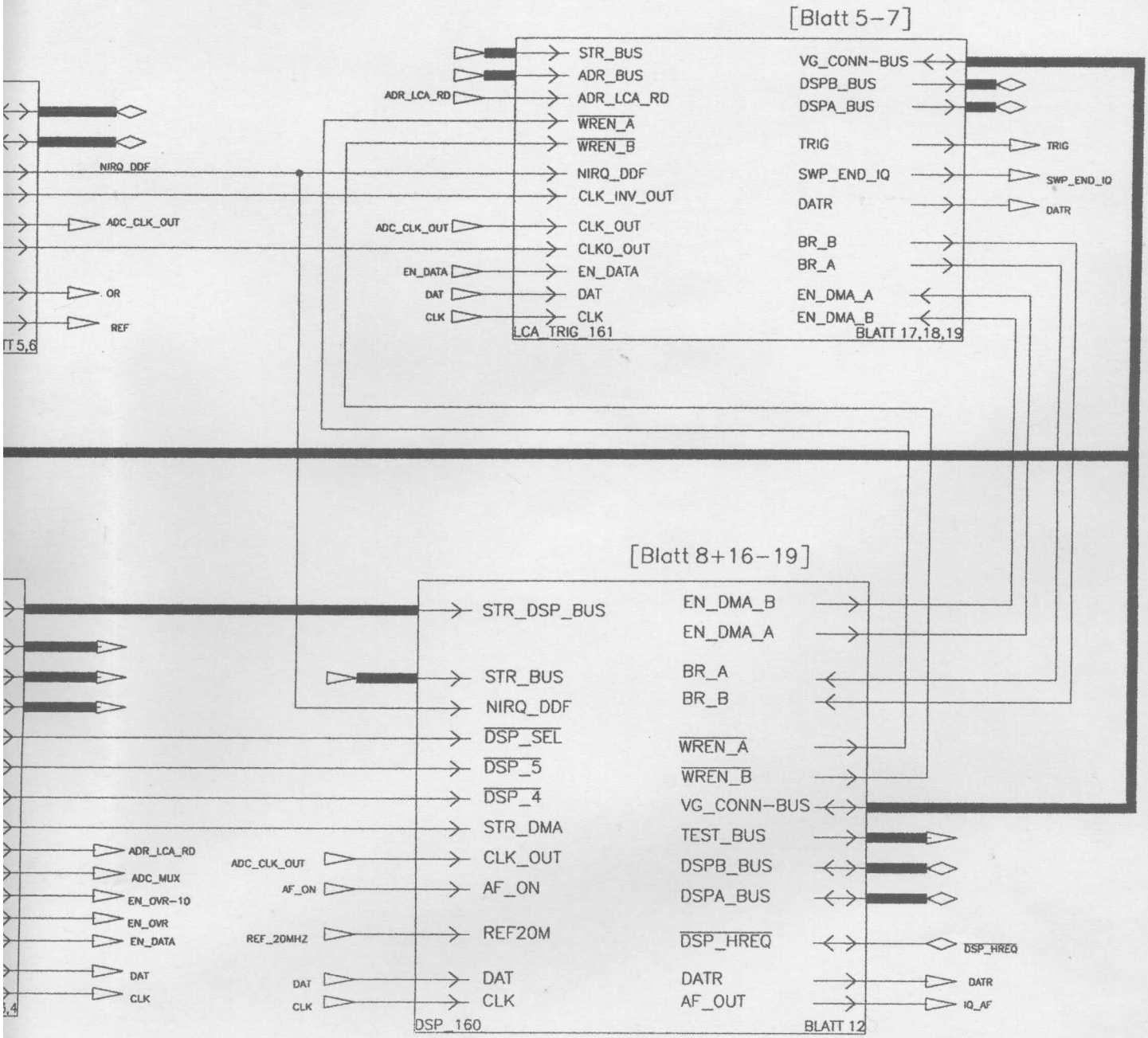
Circuit diagrams
Component plans

Schémas de circuit
Plans des composants

095.1000 Bl. 4


VG_CONN-BUS
Terminierung direkt
an VG-Leiste
X170 A1 READY
X170 B28 RXD
X170 B27 TXD
X170 B15 SC1
X170 B19 SC2
X170 B26 SCLK
X170 B16 R115 0 SCK_1
X170 B25 STD
X170 B18 SRD
X170 B20 SYNC0
X170 B11 SYNC1
X170 B21 SYNC2
X170 B12 SYNC3
X170 A7 TP_CLK
X170 C7 TP_DAT
X170 A8 TP_STR_ADR
X170 C8 TP_DATR
X170 A9 TP_CLKR
X170 C9 TP_STR_DAT
X170 C24 TP_SDA
X170 C25 TP_SCL
R322 1K GNDD
R329 1.21K GNDD
R331 1K GNDD
R343 1K GNDD
R346 432 GNDD
TEST_BUS
SWITCH_BUS
STR_BUS
ADR_BUS
OR
OR
X172 SMB-ST 1 2 3 4 5 GNDA
IF_IN
IF_IN
EN_OVR
EN_OVR
EN_OVR-10
EN_OVR-10
INTRES
INTRES
X173 SMB-ST 1 2 3 4 5 GNDA
120MHZ_IN
REF
+10V_REF
DAT
DAT
CLK
CLK
ANALOG_159
X170 A20 IF_OVR
X170 A21 IF_OVR-10
X170 A24 INTRES
X170 A25 ADC_MUX
X170 B13 DSP_HREQ
X170 C15 SWP_END_IQ
X170 C19 IQ_AF
X170 A31 B31 C31 L34 11UH C120 33U C65 100N GNDA GNDA +5VA
X170 A29 B29 C29 L12 10UH C116 100N C67 33U GNDA GNDA -15VA
X170 A30 B30 C30 L38 10UH C119 100N C118 33U GNDA GNDA +15VA
X170 C28 L10 10U C123 100N C121 10U GNDA GNDA +28VA
X170 A6 B6 C6 L31 11UH C130 100N C125 33U GNDD GNDD +5VD
X170 A2 B2 C2 GNDA
X170 A3 B3 C3 GNDA
X170 A32 B32 C32 GNDA
X170 A4 B4 C4
X170 A5 B5 C5
Z2 400B
1 2 3 4 5 6 7
GNDD
R262 0
GNDA
FUER DIESE UNTERLAGE
BEHALTEN WIR UNS ALLE RECHTE VOR


5
6
7
8
[Blatt 5,6,9–11]
EST_BUS
SWITCH_BUS
STR_BUS
ADR_BUS
IF_OUT
120MHZ_OUT
ADC_CLK
ADC_IN
ADC_CLK_INV
ADC_CLK0
REF_20MHZ
IF_OVR–10
IF_OVR
LO_ON
REF_1_2
AF_ON
BLATT 7,8,9,10,11
X178
SMB–ST
X174
SMB–ST
X171
SMB–ST
GNDA
R381
33.2
R427
200
R370
33.2
[Blatt 9–10]
ADC_CLK
ADC_IN
ADC_CLK_INV
STR_BUS
ADR_BUS
ADC_CLK0
TRIG
TRG
DAT
DAT
CLK
CLK
DIGITAL_158
DSPB_BUS
DSPA_BUS
NIRQ_DDF
ADC_CLK_INVOUT
ADC_CLK_OUT
ADC_CLK0_OUT
OR
+10V_REF
BLATT 5,6
[Blatt 3–4]
VG_CONN–BUS
TEST_BUS
LO_ON
REF_1_2
DATR
DATR
INTERFACE_157
STR_DSP_BUS
ADR_BUS
STR_BUS
SWITCH_BUS
DSP_SEL
DSP_5
DSP_4
STR_DMA
ADR_LCA_RD
ADC_MUX
EN_OVR–10
EN_OVR
EN_DATA
DAT
CLK
BLATT 3,4
ACHTUNG: EGB !
ELEKTROSTATISCH GEFAEHRDETE BAUELEMENTE ERFORDERN EINE BESONDERE HANDHABUNG.
ATTENTION ESD !
ELECTROSTATIC SENSITIVE DEVICES REQUIRE A SPECIAL HANDLING
* NICHT BESTUECKT
NOT FITTED



Hier sind noch drei hierarchische
Bloecke eingebunden

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				GEPR.		PA	I/Q_DEMODULATOR
				NORM			
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				ROHDE&SCHWARZ			ZEICHN.-NR. 1066.1260.01 S
AEND. IND.	AENDERUNGS-MITTEILUNG	DATUM	NAME	ZU GERAET FSE			REG.I.V. 1065.6000 ERSTE Z.

BLATT-NR. 2 + 19